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Doping-Free Fabrication of Carbon Nanotube Based Ballistic CMOS Devices and Circuits

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ABSTRACT

We have fabricated ballistic n-type carbon nanotube (CNT)-based field-effect transistors (FETs) by contacting semiconducting single wall CNTs using Sc. Together with the demonstrated ballistic p-type CNT FETs using Pd contacts, our work closes the gap for doping-free fabrication of CNT-based ballistic complementary metal-oxide semiconductor (CMOS) devices and circuits. We demonstrated the feasibility of this doping-free CMOS technology by fabricating a simple CMOS inverter on a SiO_2/Si substrate using the back-gate geometry, but in principle much more complicated CMOS circuits may be integrated on a CNT on any suitable insulator substrate using the top-gate geometry and high-κ dielectrics. This CNT-based CMOS technology only requires the patterning of arrays of parallel semiconducting CNTs with moderately narrow diameter range, for example, 1.6–2.4 nm, which is within the reach of current nanotechnology. This may lead to the integration of CNT-based CMOS devices with increasing complexity and possibly find its way into the computers brain: the logic circuit.

The silicon-based CMOS (complementary metal-oxide semiconductor) technology was first introduced in the 1960s and became the mainstream integrated circuit technology since the 1980s. The latest roadmap for the semiconductor industry predicts that CMOS will reach its performance limit by around 2020,[1] and this has inspired a worldwide effort to develop alternative device technologies. One of the first possible replacements to the Si transistor is carbon nanotube (CNT)-based nonclassic CMOS, which maintains the field-effect transistor (FET) principle but replaces the Si channel by a CNT.[2−4] Although the performance of p-type CNT FETs (hole carrier) has been pushed near their perfection,[5,6] technology for fabricating equally high-performing n-type CNT FETs (electron carrier) has not been developed. Here, we show that by contacting semiconducting single-walled CNTs (SWCNTs) with scandium, near perfect n-type CNT FETs can be obtained. The ON state of the n-FET behaves like a metallic conductor with a linear source to drain current−voltage ($I_{ds}-V_{ds}$) characteristic at low bias that persists down to 4.3 K and a near ballistic room-temperature conductance $G \sim 0.5G_0$ ($G_0 = 4e^2/h$), which increases with decreasing temperature. In combination with earlier developments for high-performing p-CNT FETs,[5,6] the polarity control of the CNT FETs is realized simply by choosing electrode materials, that is, Pd for p-type CNT FETs and Sc for n-type CNT FETs, thereby leading to a doping-free near ballistic CMOS technology. Although the working principles for the doping-free CMOS technology are demonstrated here using CNT-based FETs, these principles are expected to remain valid for any one-dimensional (1D) semiconductors, such as semiconducting nanowires with very small diameters.[7]

CNT is exceptional in that it has a perfect crystalline structure, which is composed of strong covalent C−C bonds, and there exists no dangling bonds on its surface.[8,9] Much progress has been made in recent years showing that CNT-based FETs can outperform the state-of-the-art silicon FETs in many ways.[2−4] In particular, room-temperature ballistic transport has been demonstrated for both metallic and semiconducting CNTs, and high-κ dielectrics have been integrated with CNT FETs.[3,10] However, the control of the electronic properties of the CNTs via doping is difficult. This is because semiconducting CNTs cannot be doped using the tranditional approach for bulk semiconductors,[2] for example,

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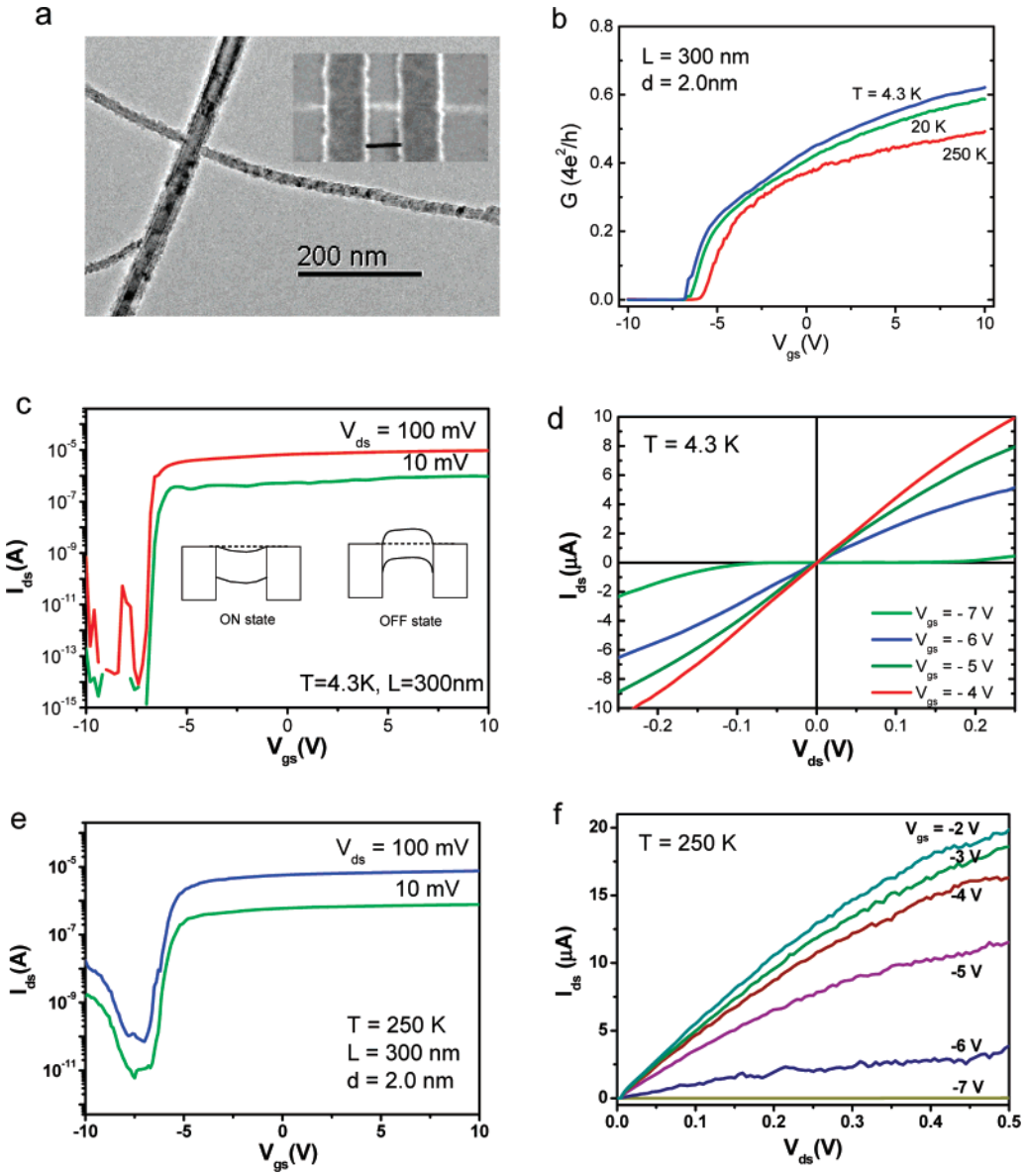

Figure 1. Back-gated SWCNT-based n-type CNT FET on a SiO_2 (100 nm)/Si substrate. (a) TEM image showing uniformly Sc-coated CNTs of various diameters; (inset) SEM image of the device, the bar is 300 nm. (b) Low bias ($V_{ds} = 0.1$ V) conductance G vs gate voltage V_{gs} for a SWCNT with a diameter $d = 2.0$ nm and a length $L = 300$ nm. The conductance increases with decreasing temperature from $0.49G_0$ at 250 K to $0.62G_0$ at 4.3 K. (c) Transfer characteristics of the same device as in b for different bias at 4.3 K; (inset) schematic ON and OFF state band diagrams for a device with zero-Schottky barrier for electron injection into the conduction band of the CNT. (d) $I_{ds}-V_{ds}$ curves for different V_{gs} and the same device as in b at 4.3 K. (e, f) Same as c and d but for different $T = 250$ K.

via ion implantation.[11] Early CNT FETs were mainly fabricated by contacting the as grown CNTs with Pt[12] and Au,[13] and the as made FETs invariably showed p-type characteristics, that is, they were ON for large negative gate bias V_{gs}. These CNT FETs were also found to be Schottky barrier (SB) devices[14] where the ON state current reduces exponentially with increasing barrier height ϕ_{SB} at the contact.[15] A breakthrough in fabricating high-performance p-type CNT FETs was made by Dai and co-workers at the Stanford University who discovered that Pd forms zero or negative SB with SWCNTs of diameters larger than about 1.6 nm and small barrier with smaller SWCNT.[5,6] The ON state of the Pd-contacted p-type CNT FET exhibits metallic-like behavior, having a room-temperature conductance that is near the ballistic transport limit of $G_0 = 4e^2/h$. While much progress has since been made in fabricating almost perfect p-type CNT FETs,[3] progress on developing high-performance n-type CNT FETs has been slow,[16−19] and in particular zero SB n-type ballistic transport has not been demonstrated for SWCNTs.

We find Sc affords almost perfect contact with the conduction band of SWCNTs and is therefore the ideal electrode material for fabricating n-type CNT FETs. In Figure 1, we show the electrical characteristics of a Sc-contacted, back-gated (silicon oxide thickness $t_{ox} = 100$ nm) semiconducting SWCNT- ($d = 2.0$ nm, $L = 300$ nm) based FET. The device is an n-type FET exhibiting ON state at large V_{gs} (~10 V) and a near ballistic ON state conductance $G_{on} = 0.49G_0$ at 250 K (Figure 1b). The ON state conductance increases with decreasing temperature and reaches $G_{on} =$

$0.62G_0$ at 4.3 K. This is typical metallic-like temperature dependent behavior, and the conductance increase[20] at lower temperature results from the reduced phonon scattering. The low-temperature (4.3 K, Figure 1d) $I_{ds}-V_{ds}$ characteristics of the ON states (with $V_{gs} > -6$ V) are almost perfectly linear at low bias. The metallic-like temperature dependence of the ON state conductance and the almost perfect linear $I_{ds}-V_{ds}$ characteristics suggest that electron injection from the Sc electrode into the conductance band of the CNT is effectively barrier free, that is, Sc forms an ohmic contact with the n-channel (i.e., the conduction band) of the CNT. At low temperature (4.3 K, Figure 1c), the I_{on}/I_{off} ratio exceeds 10^9 for $V_{ds} = 0.1$ V, and this ratio remains larger than 10^5 at 250 K (Figure 1e). The ON state current of the device at 250 K and under $V_{gs} = -2$ V reaches 20 μA (Figure 1f). When normalized by the width of the CNT channel ($d = 2$ nm), this not fully saturated ON state current reaches about 10 ,000 μA/μm. This ON state current and the relevant threshold swing $S = 250$ mV/dec ($V_{ds} = 0.1$ V, $T = 250$ K, Figure 1e) are comparable to that of the best Pd-contacted p-type CNT FETs after normalized by the conduction channel width (for the ON state current) and oxide thickness (for S).[3,5]

While it is difficult to form ohmic contacts to intrinsic planar Si channels due to the Fermi-level pinning,[11] for a 1D channel such as a CNT, Fermi-level pinning at the metal−CNT interface is weak.[2,21] This is because in a 1D channel any interface states-induced potential change (due to, e.g., interface dipoles) decays to zero rapidly in regions away from the interface. The SB formed at the metal−CNT interface is thus much thinner than that in 3D and carrier tunneling through the SB is important in CNT devices. The SB height is primarily governed by the energy difference between the Fermi level of the metal electrode and the position of the valence (p-type) or conduction (n-type) band edge of the CNT. A metal with a large work function, for example, Pt (5.65 eV), Au (5.1 eV), or Pd (5.1 eV), thus tends to line-up with the valence band of the CNT and forms a p-channel for hole transport through the CNT. On the other hand, a metal with a small work function, for example, Sc (3.3 eV) or Ca (2.9 eV),[22] tends to line-up with the conduction band of the CNT and forms an n-channel for electron injection from the metal electrode into the CNT. However, the work function is not the only factor determining the SB formed at the metal−CNT interface.[2] In particular, the bonding configuration of the metal atoms and wetting[3] on the CNT are expected to affect significantly the transport behavior of the CNT. The excellent performance of the Sc-contacted n-type CNT FET results from several favorable factors, including suitable low work function, the expected covalent bonding,[23] and excellent wetting with the CNT (Figure 1a).

The control of the majority carrier type in a semiconducting CNT channel, that is, electron (n-type) or hole (p-type), is realized here by the selective injection of electrons or holes into the CNT. For a Pd-contacted CNT, the Fermi-level of the Pd electrode aligns well with the valence band of the CNT,[5] affording near ballistic p-channel conductance. For a

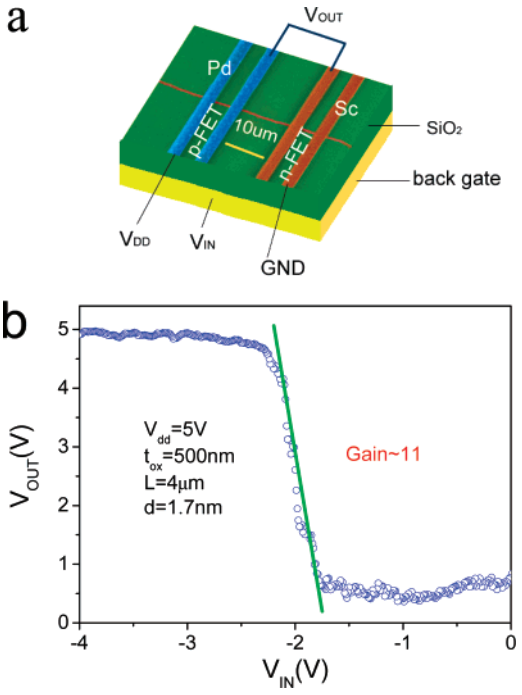

Figure 2. Back-gated ($t_{ox} = 500$ nm) SWCNT complementary inverter. (a) SEM image of a SWCNT-based complementary inverter involving a p- and an n-type CNT FETs fabricated on the same SWCNT. The polarity of the CNT FET is controlled by the injection of carriers to the valence band (hole carrier and p-type) and conduction band (electron carrier and n-type) using Pd (p-type) or Sc (n-type) electrodes. (b) Transfer characteristic for a complementary SWCNT-based inverter with a CNT diameter $d = 1.7$ nm and a source-drain channel length $L = 4$ μm.

Sc-contacted CNT, we find that the Fermi-level of the Sc electrode aligns well with the conductance band of the CNT, affording near ballistic n-channel conductance and large ON state current (Figure 1b). When a long intrinsic semiconducting CNT (i-CNT, Figure 2a) is contacted alternatively with Pd and Sc electrodes, both p- and n-type FETs may be fabricated and in principle high efficient ballistic CMOS circuits may be integrated on a single CNT without intentional doping and therefore associated inhomogeneities along the CNT channel. A complementary NOT logic, that is, inverter, is shown in Figure 2a for a back-gate geometry. The inverter represents the simplest CMOS circuit. Figure 2a shows that the CNT CMOS inverter consists of an n-type and a p-type CNT FET, and these CNT FETs are fabricated simply by contacting the CNT channel using Pd (p-type) and Sc (n-type) electrodes. The input voltage for the inverter is provided by the common back-gate voltage $V_{IN} = V_{gs}$ of both the n- and p-type CNT FETs, while the output of the inverter is read from the common drain terminals. The voltage transfer characteristic of the inverter (Figure 2b) shows a voltage gain of $\beta = \Delta V_{out}/\Delta V_{in} = 10.8$. This is among the highest gains obtained for back-gated devices with SiO_2 being the gate oxide,[17] although a rather thick (500 nm) gate oxide layer is used in this work.

The CNTs used in this work are long SWCNTs of a few hundred micrometers in length, which were directionally grown on heavily n-doped silicon substrate covered with a layer of insulating SiO_2 via catalytic chemical vapor deposi-

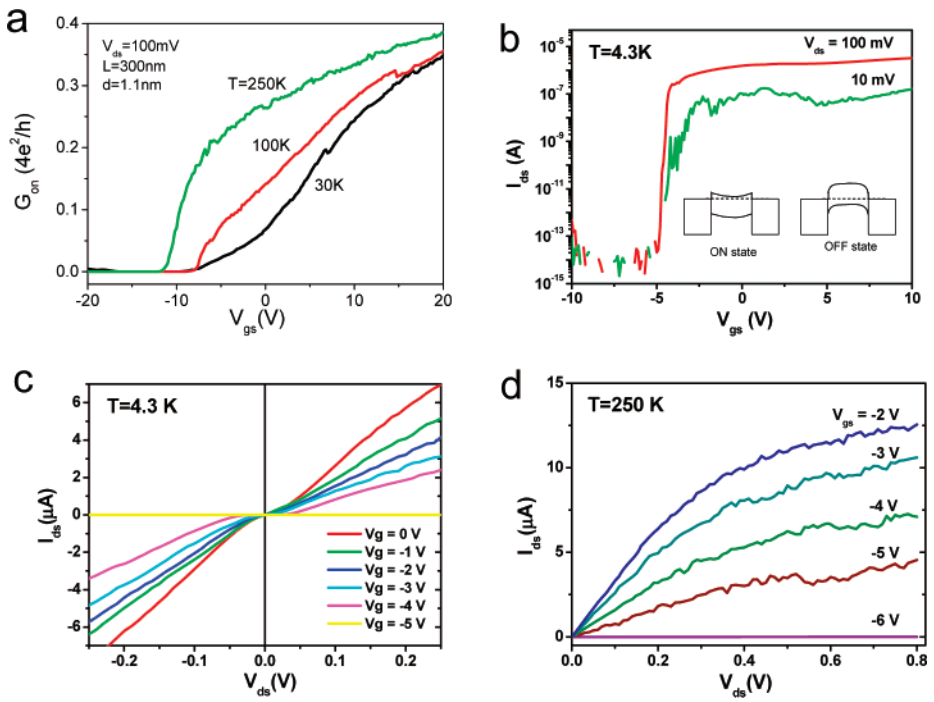

Figure 3. Electrical characteristics of a small SWCNT- (with $d = 1.1$ nm, $L = 300$ nm) based n-type FET. (a) Low-bias conductance vs gate voltage V_{gs} recorded at various temperatures. (b) Transfer characteristics of the device at 4.3 K; (inset) schematic ON and OFF state band diagrams for the device with a small Schottky barrier for electron injection. (c) Low bias $I_{ds}-V_{ds}$ vs V_{gs} for the device at 4.3 K. There exists a small nonlinear region near zero bias suggesting the existence of a small Schottky barrier between the Sc electrode and the SWCNT of small diameter. (d) $I_{ds}-V_{ds}$ characteristics at 250 K for different V_{gs}.

tion.[24,25] Although it is still not possible to grow SWCNTs with predefined chirality,[26] with carefully controlled growth conditions it is possible to grow a long SWCNT with the same chirality. Because our CNT-based CMOS technology does not require doping the CNT, the electronic properties may then be made uniform along the long intrinsic CNT, and in principle a CNT-based CMOS circuit of moderate complexity, such as a CNT ring oscillator[27] or a configurable macro cell in a field programmable gate arrays structure,[28] may be integrated on the same CNT. The desired logical functions may be realized by connecting the inputs and outputs of the macro cells to external wiring channels, thus establishing direct connections between the outputs of one macro cell to the input of other macro cells or I/O-blocks.

While the CNT-based CMOS technology is compatible with the Si-based CMOS technology as demonstrated in this work, it does not rely on the use of SiO_2 and Si substrate. In principle, any suitable insulating substrate[29] may be used to support the CNTs, and the only requirement of the CNT-based CMOS technology is the patterning of arrays of parallel semiconducting CNTs with suitable spacing and diameters, for example, between 1.6−2.4 nm on an insulating substrate. While the fabrication of even the simplest Si-based CMOS inverter involves more than ten complicated processing steps, the fabrication of CMOS circuits using CNTs on an insulating substrate involves basically only three steps, that is, patterning and (1) deposition of gate oxide (for example, high-κ dielectric), (2) deposition of Pd contacts and gates for p-type CNT FETs, and (3) deposition of Sc contacts and gates for n-type CNT FETs. The symmetric CNT band structure about the Fermi level results in an additional advantage for CNT-based CMOS technology, that is, the effective masses for hole and electron are the same in CNT leading to near symmetric hole and electron transport, while the effective electron mobility in Si is roughly twice that of the hole making the design and fabrication of Si-based CMOS circuits more complicated.

The band gap of a semiconducting CNT depends on its diameter ($\sim 1/d$). The conduction band edge position of a CNT and thus the height of the SB formed at the metal−CNT interface are expected also to depend on d.[6,15] For p-type CNT FETs, it was shown[6,15] that the SB height ϕ_{SB} saturates almost to a constant value for $d > 1.5$ nm, but it increases with decreasing diameter of the CNT. When Sc is contacted to a small CNT ($d = 1.1$ nm, $L = 300$ nm, Figure 3) the low bias ON state conductance G_{on} of the Sc-contacted n-type CNT FET decreases with decreasing temperature from $0.39G_0$ at 250 K to $0.35G_0$ at 30 K (Figure 3a). At lower temperature (4.3 K, Figure 3c) the $I_{ds}-V_{ds}$ characteristics become nonlinear at low bias instead of linear as at $T >$ 150 K (see Supporting Information, Figure S1). The fact that the ON state conductance decreases with decreasing temperature is suggestive of thermionic injection of electrons into the CNT, and the nonlinear $I_{ds}-V_{ds}$ characteristics at low temperature show clearly that there exists a small barrier (about 4 meV for the ON state, see Supporting Information, Figure S2) for the electron injection into the CNT. Nevertheless, this small barrier does not affect significantly the performance of the n-type CNT FET at room temperature, and a current of more than 12 μA is obtained for $V_{gs} = -2$ V at 250 K (Figure 3d). Measurements on Sc-contacted p-type CNT FETs of different diameters show that Sc may

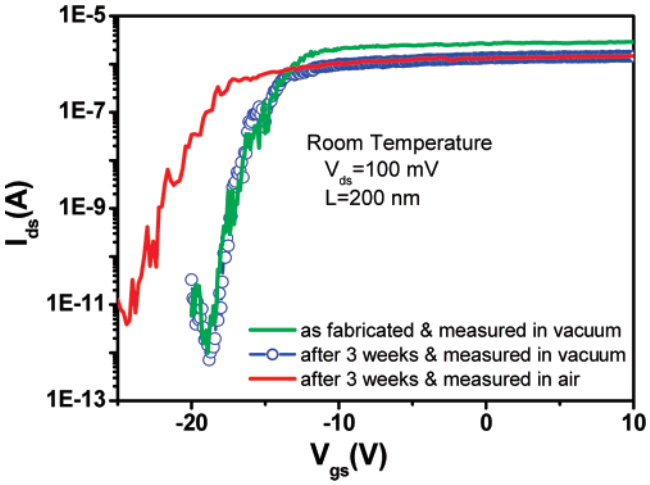

Figure 4. Transfer characteristics for a Sc-contacted n-type CNT FET. The device is based on a SWCNT with $d = 1.2$ nm and $L =$ 200 m. The green curve was measured in vacuum immediately after the device was fabricated. The device was then exposed in air for three weeks without any passivation treatment and protection and was then measured in vacuum (blue circles) and in air (red curve). The transfer characteristic of the n-type CNT FET is stable against exposition to air, except that the ON state current was reduced from 3 to 1.5 μA after three weeks.

form near ohmic contacts to SWCNTs with d being larger than about 1.5 nm resulting in a large ON state current of about 20 μA (see Supporting Information, Figure 3), and the ON state current decreases to become less than 15 μA for tube diameter of less than 1.5 nm. This diameter dependent behavior of the ON state current observed here for the Sc-contacted CNT FETs is similar to that observed for the Pd-contacted p-type CNT FETs.[17]

Practical applications of CNT-based CMOS technology require that the fabrication processes are simple involving as few steps as possible and that the performance of the fabricated devices is robust and stable. Earlier attempts on fabricating high-performance n-type CNT FETs involved either chemical doping by K[16] or annealing in vacuum,[17] but the so fabricated n-type devices are not stable and may readily recover to p-type behavior upon exposition to air. The effects of environment on the Sc-contacted n-type CNT FETs were investigated and results for a typical device are shown in Figure 4. The transfer characteristic of the device was measured in vacuum ($\sim 10^{-8}$ Torr) immediately after the device was fabricated (green curve). The room-temperature ON state current of this n-type CNT FET reaches about 3 μA for a bias of $V_{ds} = 0.1$ V and the I_{on}/I_{off} ratio exceeds 10^6. The device was kept in air without any passivation treatment for three weeks, and the device transfer characteristic was then measured in vacuum (blue circles) and in air (red curve). The characteristic of the device around the OFF state at about $V_{gs} = -19$ V is not affected significantly by three weeks exposition to air, but the ON state current at $V_{gs} > 0$ V is reduced from 3 to 1.5 μA. When the measurement was carried out in air, the transfer characteristic is significantly shifted toward lower V_{gs} by about 4 V, signifying the effect of the environment on the device. The Sc-contacted FETs also show good uniformity among devices fabricated on the same SWNT. These devices are all n-type, and their ON state current are of the same order of magnitude (see Supporting Information, S4).

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Supporting Information Available: Materials and methods and supplementary figures. This material is available free of charge via the Internet at http://pubs.acs.org.

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